In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first buffer coupled to said first component, said first buffer receiving and storing data received from said first component at said first clock rate;

a second buffer coupled to said second component, said second buffer supplying data recalled therefrom to said second component at said second clock rate;

a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.

2. (Original) The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are random-access memories.

3. (Original) The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are shift registers.

4. (Original) The circuit as set forth in Claim 1, wherein said circuit is integrated onto a semiconductor die with one of said first component or said second component.

5 to 14. (Canceled)